



LCD (COG)

型 号 : ZX12864- 0 5
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ZX12864-05完全兼容香港精电的MOBI2006液晶模组，同时，经过改进，完全避免别的厂家仿制时候出现的开机画面反显，或者开机界面翻转180度显示问题。在中显液晶模组上完全解决，欢迎大家试用！

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1. 简介

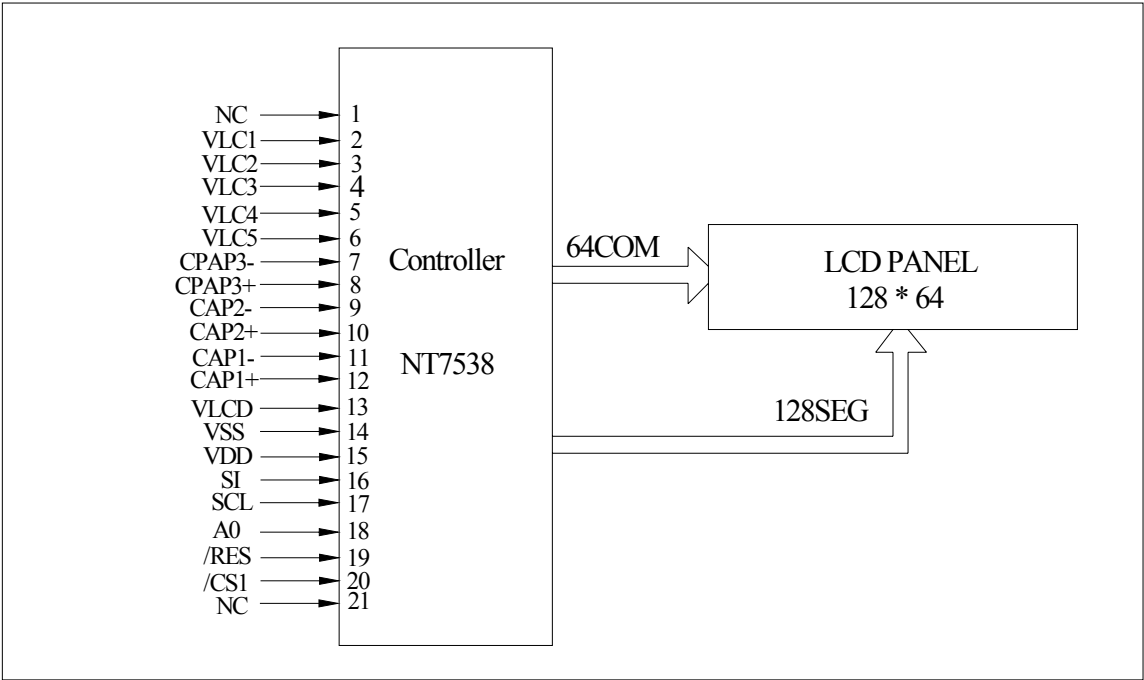
1.1 LCD 规格

项目	规格
显示类型	FSTN/正性/半透
颜色	显示像素: 黑色
	显示背景: 白色
数据输入	4-wire 串口
工作电压	8.7V (LCD) ,3.0V(VDD)
驱动方式	1/64 DUTY,1/9 BIAS
视角	6 点
控制器	NT7538(COG)
其他	

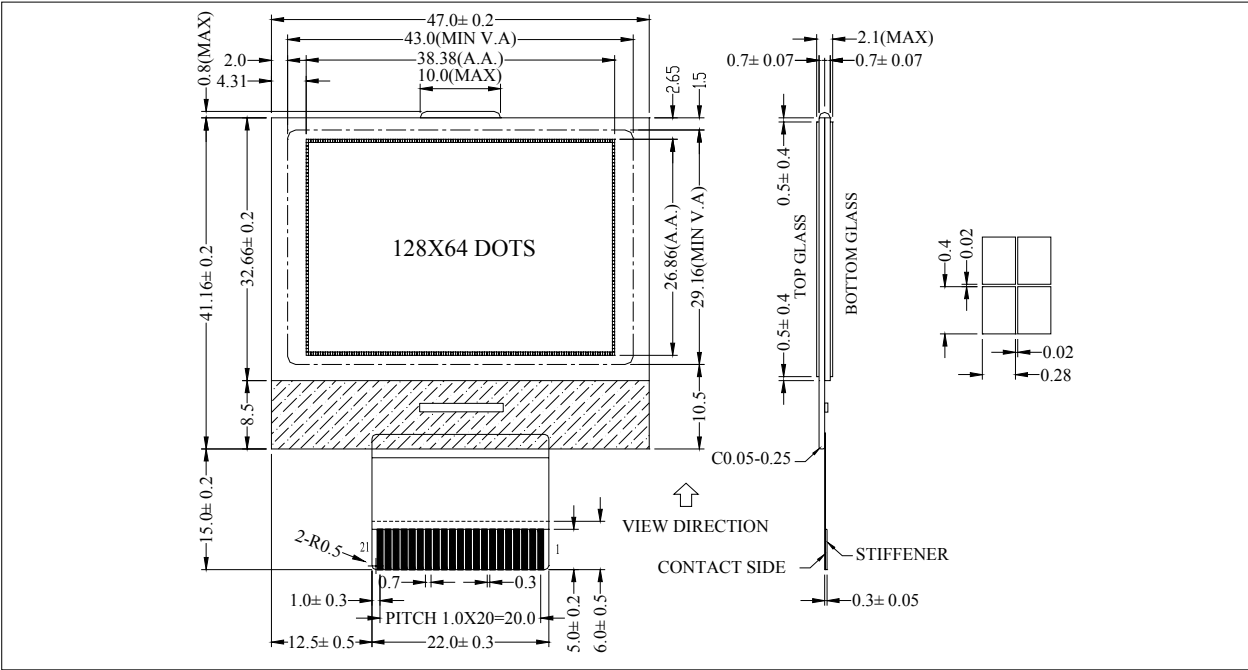
1.2 尺寸规格

项目	规格	单位	备注
LCD 尺寸	47.00(W) x 56.16(H) x 2.1Max(T)	mm	
可视区	43.00Min(w) x 29.16Min(H)	mm	
有效区	38.38(W) x 26.86(H)	mm	
点阵	128 x 64Dots	---	
点距离	0.30(W) x 0.42(H)	mm	
点大小	0.28(W) x 0.40(H)	mm	

1.3 原理结构图



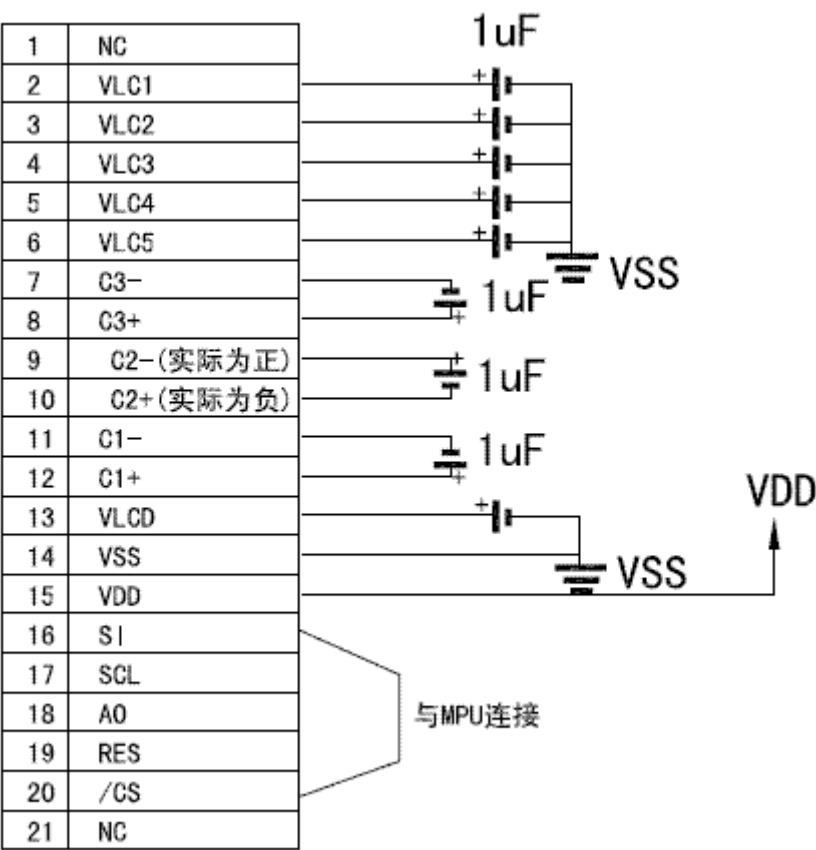
1.4 LCD 外形图



1.5 引脚定义

编号	符号	功能
1	NC	空脚
2	VLC1	LCD 驱动电压
3	VLC2	
4	VLC3	
5	VLC4	
6	VLC5	
7	CAP3-	接入一个电容，电容另一端与 CAP3+连接
8	CAP3+	接入一个电容，电容另一端与 CAP3-连接
9	CAP2-	接入一个电容，电容另一端与 CAP2+连接
10	CAP2+	接入一个电容，电容另一端与 CAP2-连接
11	CAP1-	接入一个电容，电容另一端与 CAP1+连接
12	CAP1+	接入一个电容，电容另一端与 CAP1-连接
13	VLCD	LCD 显示电压，此引脚与 VSS 之间需接一个电容
14	VSS	接地
15	VDD	逻辑电压：+3.0V
16	SI	串行数据输入
17	SCL	串行时钟输入
18	A0	H: 数据 L: 指令
19	/RES	复位信号，低有效
20	/CS1	片选信号
21	NC	空脚

1.6 四倍压电路，VDD=2.2-3.3V



*注意：电容可采用陶瓷电容，使用有极性的电容需注意电容的正负关系。

2. 极限参数

参量	符号	范围	单位
电源电压	$V_{DD}-V_{SS}$	-0.3 ~ 3.6	V
LCD 驱动电压	$V_{DD} \sim V_0$	-0.3 ~ 13.5	V
输入电压	V_{IN}	$V_{SS} \sim V_{DD}$	V
工作温度	T_{opr}	-20 ~ 70	°C
存储温度	T_{stg}	-30 ~ 80	°C

3. 电气特性

3.1 电特性

(Ta=25 °C, VSS=0V)

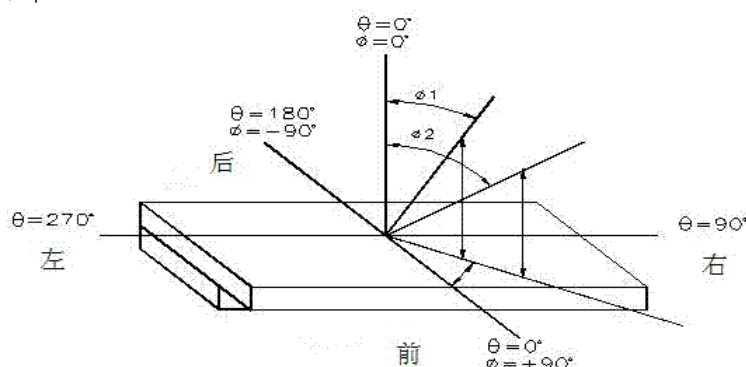
项目	符号	条件	最小值	典型值	最大值	单位	备注
逻辑工作电压	$V_{DD}-V_{SS}$	--	2.5	3.0	3.3	V	
输入高电平	V_{IH}	--	0.8 V_{DD}	--	V_{DD}	V	
输入低电平	V_{IL}	--	GND	--	0.2 V_{DD}	V	
输出高电平	V_{OH}	--	0.8 V_{DD}	--	V_{DD}	V	
输出低电平	V_{OL}	--	GND	--	0.2 V_{DD}	V	
逻辑工作电流	I_{DD}	$V_{DD}-V_{SS}=3.0V$	--	--	--	uA	
LCD 驱动电压	V_0-V_{SS} $\Phi=0$ $\theta=0$	Ta=25 °C	--	8.7	--	V	

3.2 光特性

(Ta=25 °C, $V_{DD}=3.0V$)

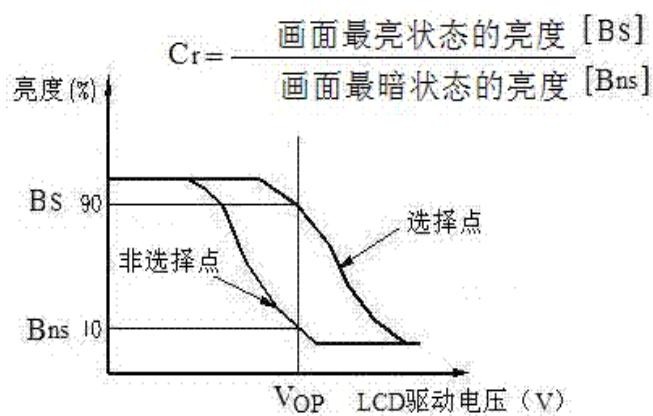
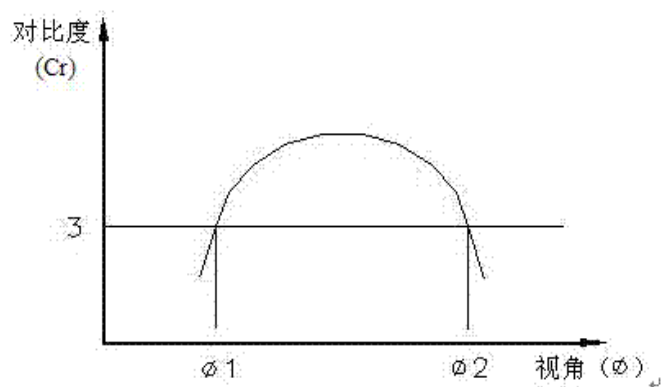
项目	符号	条件	最小值	典型值	最大值	单位	备注
视角	$\phi_2-\phi_1$	$K \geq 3$	--	50	--	DEG	1、2
对比度	K	$\phi=0^\circ, \theta=0^\circ$	3	5	--	--	3
帧频率				70		Hz	
响应时间	Tr(rise)	$\phi=0^\circ, \theta=0^\circ$	--	250	350	ms	4
	Tf(fall)	$\phi=0^\circ, \theta=0^\circ$	--	250	350	ms	

备注:

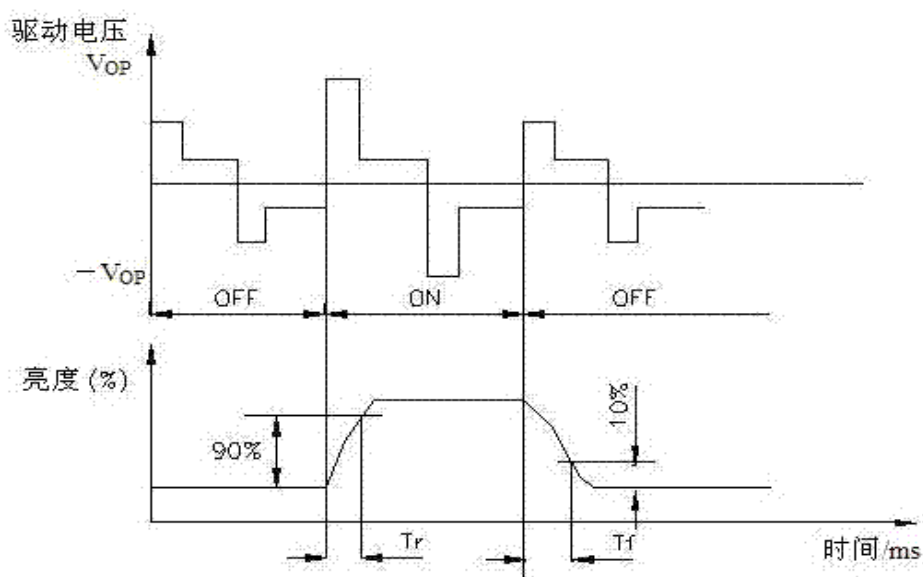
1: 视角 θ, ϕ 的定义:

2: 视角范围的定义 $\Delta\phi = |\phi_2 - \phi_1|$

3: 对比度的定义

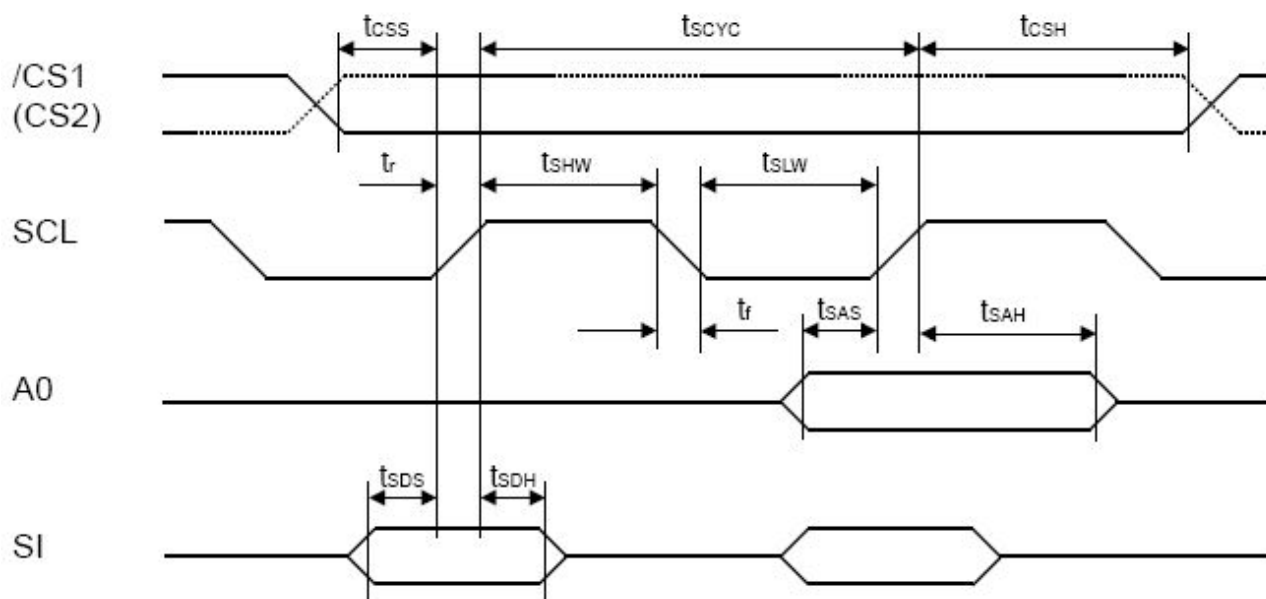


4: 响应时间的定义



4. 时序特性

4-wire 串口时序:



(VDD = 2.7 ~ 3.6V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{SCYC}	Serial clock cycle	120	-	-	ns	SCL
t_{SHW}	Serial clock H pulse width	60	-	-	ns	SCL
t_{SLW}	Serial clock L pulse width	60	-	-	ns	SCL
t_{SAS}	Address setup time	30	-	-	ns	A0
t_{SAH}	Address hold time	20	-	-	ns	A0
t_{SDS}	Data setup time	30	-	-	ns	SI
t_{SDH}	Data hold time	20	-	-	ns	SI
t_{CSS}	Chip select setup time	20	-	-	ns	$\overline{\text{CS1}}$, CS2
t_{CSH}	Chip select hold time	40	-	-	ns	$\overline{\text{CS1}}$, CS2

(VDD = 1.8 ~ 2.7V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{SCYC}	Serial clock cycle	200	-	-	ns	SCL
t_{SHW}	Serial clock H pulse width	80	-	-	ns	SCL
t_{SLW}	Serial clock L pulse width	80	-	-	ns	SCL
t_{SAS}	Address setup time	60	-	-	ns	A0
t_{SAH}	Address hold time	30	-	-	ns	A0
t_{SDS}	Data setup time	60	-	-	ns	SI
t_{SDH}	Data hold time	60	-	-	ns	SI
t_{CSS}	Chip select setup time	40	-	-	ns	$\overline{\text{CS1}}$, CS2
t_{CSH}	Chip select hold time	100	-	-	ns	$\overline{\text{CS1}}$, CS2

*1. The input signal rise time and fall time (t_r , t_f) is specified as 15ns or less.

*2. All timing is specified using 20% and 80% of VDD as the standard.

5. 控制器指令及功能介绍

Commands

The NT7538 uses a combination of A0, /RD (E) and /WR (R/W) signals to identify data bus signals. As the chip analyzes and executes each command using internal timing clock only regardless of external clock, its processing speed is very high and its busy check is usually not required. The 8080 series microprocessor interface enters a read status when a low pulse is input to the /RD pad and a write status when a low pulse is input to the /WR pad. The 6800 series microprocessor interface enters a read status when a high pulse is input to the R/W pad and a write status when a low pulse is input to this pad. When a high pulse is input to the E pad, the command is activated. (For timing, see AC Characteristics.). Accordingly, in the command explanation and command table, /RD (E) becomes 1(high) when the 6800 series microprocessor interface reads status of display data. This is the only different point from the 8080 series microprocessor interface.

Taking the 8080 series microprocessor interface as an example, commands are explained below. When the serial interface is selected, input data starting from D7 in sequence.

1. Display ON/OFF

Alternatively turns the display on and off.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Setting
0	1	0	1	0	1	0	1	1	1	1	AFh	Display ON
										0	AEh	Display OFF

When the display OFF command is executed when in the display all points ON mode, power save mode is entered. See the section on the power saver for details.

2. Display Start Line Set

Specifies line address (refer to Figure 6) to determine the initial display line, or COM0. The RAM display data becomes the top line of LCD screen. The higher number of lines in ascending order, corresponding to the duty cycle follows it. When this command changes the line address, smooth scrolling or a page change takes place.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	0	1	A5	A4	A3	A2	A1	A0	40h to 7Fh

A5	A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
			:			:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

3. Page Address Set

Specifies page address to load display RAM data to page address register. Any RAM data bit can be accessed when its page address and column address are specified. The display remains unchanged even when the page address is changed. Page address 8 is the display RAM area dedicated to the indicator, and only D0 is valid for data change.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
/RD		/WR									
0	1	0	1	0	1	1	A3	A2	A1	A0	B0h to B8h

A3	A2	A1	A0	Page address
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
		:		:
0	1	1	1	7
1	0	0	0	8

4. Column Address Set

Specifies column address of display RAM. Divide the column address into 4 higher bits and 4 lower bits. Set each of them succession. When the microprocessor repeats to access the display RAM, the column address counter is incremental by during each access until address 132 is accessed. The page address is not changed during this time.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
/RD		/WR									
0	1	0	0	0	0	1	A7	A6	A5	A4	10h to 18h
						0	A3	A2	A1	A0	00h to 0Fh

High nibble

Low nibble

A7	A6	A5	A4	A3	A2	A1	A0	Column address
0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	1	1
0	0	0	1	0	1	1	0	2
			:					:
1	0	0	0	0	0	1	0	130
1	0	0	0	0	0	1	1	131

5. Read Status

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0
/RD	/WR									
0	0	1	BUSY	/ADC	OFF/ON	RESET	0	0	0	0

BUSY: When high, the NT7538 is busy due to internal operation or reset. Any command is rejected until BUSY goes low. The busy check is not required if enough time is provided for each cycle.

/ADC: Indicates the relationship between RAM column address and segment drivers. When low, the display is reversed and column address "131-n" corresponds to segment driver n. when high, the display is normal and column address corresponds to segment driver n.

OFF/ON: Indicates whether the display is on or off. When low, the display turns on. When high, the display turns off. This is the opposite of Display ON/OFF command.

RESET: Indicates the initialization is in progress by /RES signal or by reset command. When low, the display is on. When high, the chip is being reset.

6. Write Display Data

Write 8-bit data in display RAM. As the column address automatically increments by 1 after each write, the microprocessor can continue to write data of multiple words.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0
/RD	/WR									
1	1	0	Write Data							

7. Read Display Data

Reads 8-bit data from display RAM area specified by column address and page address. As the column address automatically increments by 1 after each write, the microprocessor can continue to read data of multiple words. A single dummy read is required immediately after column address setup. Refer to the display RAM section of FUNCTIONAL DESCRIPTION for details. Note that no display data can be read via the serial interface.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0
/RD	/WR									
1	0	1	Read Data							

8. ADC Select

Changes the relationship between RAM column address and segment driver. The order of segment driver output pads could be reversed by software. This allows flexible IC layout during LCD module assembly. For details, refer to the column address section of Figure 4. When display data is written or read, the column address is incremented by 1 as shown in Figure 4.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Setting
/RD	/WR											
0	1	0	1	0	1	0	0	0	0	0	A0h	Normal
										1	A1h	Reverse

9. Normal/ Reverse Display

Reverses the Display ON/OFF status without rewriting the contents of the display data RAM.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Setting
0	1	0	1	0	1	0	0	1	1	0	A6h	RAM Data "H" LCD ON voltage (normal)
										1	A7h	RAM Data "L" LCD ON voltage (reverse)

10. Entire Display ON

Forcibly turns the entire display on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held. This command has priority over the Normal/Reverse Display command. When D is low, the normal display status is provided.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Setting
0	1	0	1	0	1	0	0	1	0	0	A4h	Normal display mode
										1	A5h	Display all points ON

When D0 is high, the entire display ON status is provided. If the Entire Display ON command is executed in the display OFF status, the LCD panel enters Power save mode. Refer to the Power Save section for details.

11. LCD Bias Set

This command selects the voltage bias ratio required for the liquid crystal display.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Duty		
												1/33	1/49	1/65
0	1	0	1	0	1	0	0	0	1	0	A2h	1/6 bias	1/8 bias	1/9 bias
										1	A3h	1/5 bias	1/6 bias	1/7 bias

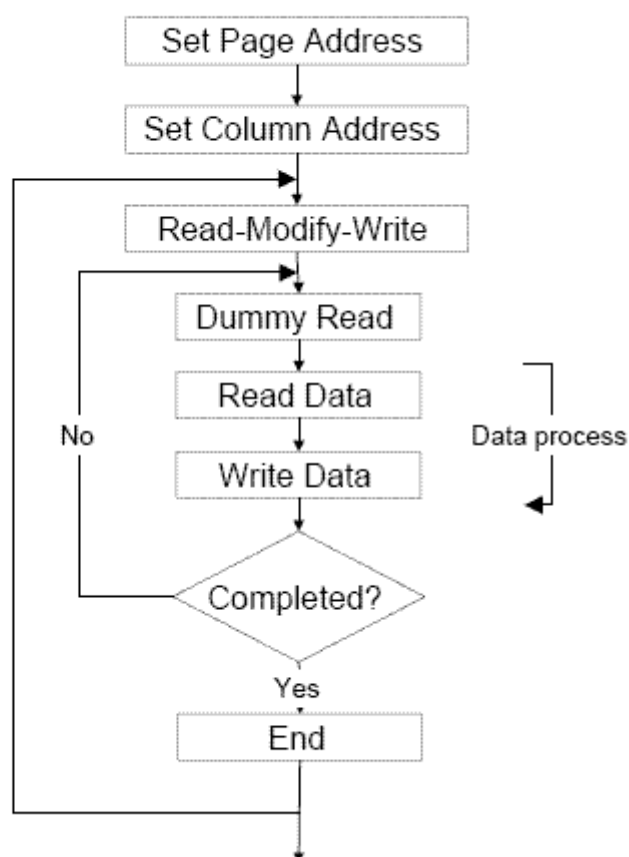
12. Read-Modify-Write

A pair of Read-Modify-Write and End commands must always be used. Once Read-Modify-Write is issued, column address is not incremental by Read Display Data command but incremental by Write Display Data command only. It continues until End command is issued. When the End is issued, column address returns to the address when Read-Modify-Write is issued. This can reduce the microprocessor load when data of a specific display area is repeatedly changed during cursor blinking or other events.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	1	1	0	0	0	0	0	E0h

Note: Any command except Read/Write Display Data and Column Address Set can be issued during Read-Modify-Write mode.

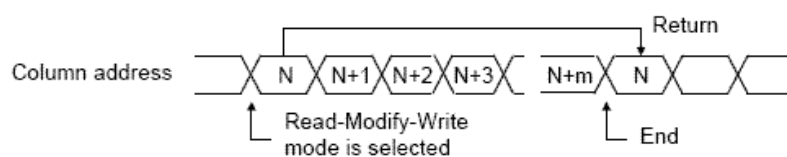
Cursor display sequence



13. End

Cancels Read-Modify-Write mode and returns column address to the original address (when Read-Modify-Write is issued)

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
	/RD	/WR									
0	1	0	1	1	1	0	1	1	1	0	EEh



14. Reset

This command resets the Display Start Line register, Column Address counter, Page Address register, and Common output mode register, the V0 voltage regulator internal resistor ratio register, the Electronic Volume register, the static indicator mode register, the read-modify-write mode register, and the test mode. The Reset command does not affect on the contents of display RAM. Refer to the Reset circuit section of Function Description.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	1	1	0	0	0	1	0	E2h

The Reset command cannot initialize LCD power supply. Only the Reset signal to the /RES pad can initialize the supplies.

15. Output Status Select Register

When D3 is high or low, the scan direction of the COM output pad is selectable. Refer to Output Status Selector Circuit in Function Description for details.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	1	0	0	0	*	*	*	C0h to C7h
							1				C8h to CFh

*: Invalid bit

D3 = 0: Normal (COM0 → COM63/47/31)

D3 = 1: Reverse (COM63/47/31 → COM0)

16. Power Control Set

Select one of eight power circuit functions using 3-bit register. An external power supply and part of on-chip power circuit can be used simultaneously. Refer to Power Supply Circuit section of FUNCTIONAL DESCRIPTION for details.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	0	0	1	0	1	A2	A1	A0	28h to 2Fh

When A0 goes low, voltage follower turns off. When A0 goes high, it turns on.

When A1 goes low, voltage regulator turns off. When A1 goes high, it turns on.

When A2 goes low, voltage booster turns off. When A2 goes high, it turns on.

17. V0 Voltage Regulator Internal Resistor Ratio Set

This command sets the V0 voltage regulator internal resistor ratio. For details, see explanation under "The Power Supply Circuits".

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Rb/Ra Ratio
0	1	0	0	0	1	0	0	0	0	0	20h	Small
								0	0	1	21h	
								0	1	0	22h	
											:	
								1	1	0	26h	
								1	1	1	27h	Large

18. The Electronic Volume (Double Byte Command)

This command makes it possible to adjust the brightness of the liquid crystal display by controlling the liquid crystal drive voltage V0 through the output from the voltage regulator circuits of the internal liquid crystal power supply. It is a two-byte command used as a pair with the electronic volume mode set command and the electronic volume register set command, and both commands must be issued one after the other.

(1) The Electronic Volume Mode Set

When this command is input, the electronic volume register set command is enabled. Once the electronic volume mode has been set, no other command except for the electronic volume register command can be used. Once the electronic volume register set command has been used to set data into the register, then the electronic volume mode is released.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	0	0	0	0	0	0	1	81h

(2) Electronic Volume Register Set

By using this command to set six bits of data to the electronic volume register, the liquid crystal voltage V0 assumes one of the 64 voltage levels. When this command is input, the electronic volume mode is released after the electronic volume register has been set.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex	V0
0	1	0	*	*	0	0	0	0	0	1	XX	Small
					0	0	0	0	1	0	XX	
									:		:	:
					1	1	1	1	1	0	XX	
					1	1	1	1	1	1	XX	Large

When the electronic volume function is not used, set D5 - D0 to 100000.

19. Static Indicator (Double Byte Command)

This command controls the static drive system indicator display. The static indicator display is controlled by this command only, and is independent of other display control commands.

This is used when one of the static indicator liquid crystal drive electrodes is connected to the FR terminal, and the other is connected to the FRS terminal. A different pattern is recommended for the static indicator electrodes than for the dynamic drive electrodes. If the pattern is too close, it can result in deterioration of the liquid crystal and of the electrodes.

The static indicator ON command is a double bytes command paired with the static indicator register set command, and thus command must be executed one after the other. (The static indicator OFF command is a single byte command)

(1) Static Indicator ON/OFF

When the static indicator ON command is entered, the static indicator register set command is enabled. Once the static indicator ON command has been entered, no other command aside from the static indicator register set command can be used. This mode is cleared when data is set in the register by the static indicator register set command.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Setting
0	1	0	1	0	1	0	1	1	0	0	ACh	Static Indicator OFF
										1	ADh	Static Indicator ON

(2) Static Indicator Register Set

This command sets two bits of data into the static indicator register and used to set the static indicator into a blinking mode.

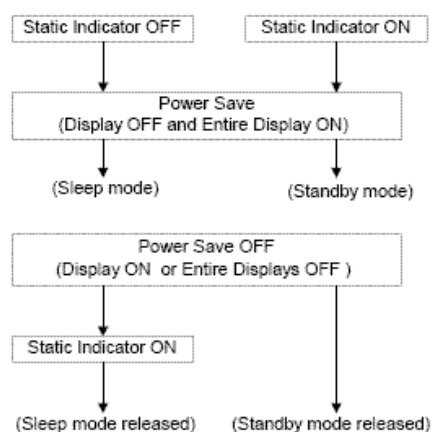
A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Indicator Display Status
0	1	0	*	*	*	*	*	*	0	0	XX	OFF
									0	1	XX	ON (blinking at approximately 1 second intervals)
									1	0	XX	ON (blinking at approximately 0.5 second intervals)
									1	1	XX	ON (constantly on)

20. Power Save (Compound Command)

When all displays are turned on during display off, the Power Save command is issued to greatly reduce current consumption.

If the static indicator is off, the Power Save command makes the system enter sleep mode. If the static indicator is on, this command makes the system enter standby mode.

Release the Sleep mode using the both Power Save OFF command (Display ON command or Entire Display OFF command) and Set Indicator On command.



Sleep Mode

This mode stops every operation of the LCD display system, and can reduce current consumption nearly to a static current value if no access is made from the microprocessor. The internal status in the sleep mode is as follows:

- (1) Stops the oscillator circuit and LCD power supply circuit.
- (2) Stops the LCD driver and outputs the VSS level as the segment/common driver output.
- (3) Holds the display data and operation mode provided before the start of the sleep mode.
- (4) The MPU can access the built-in display data RAM.

Standby Mode

Stops the operation of the duty LCD displays system and turns on only the static drive system to reduce current consumption to the minimum level required for static drive. The ON operation of the static drive system indicates that the NT7538 is in standby mode. The internal status in the standby mode is as follows:

- (1) Stops the LCD power supply circuit.
- (2) Stops the LCD drive and outputs the VSS level as the segment / common driver output.
However, the static drive system still operates.
- (3) Holds the display data and operation mode provided before the start of the standby mode.
- (4) The MPU can access the built-in display data RAM.

When the Reset command is issued in the standby mode, the sleep mode is set.

- When the LCD drive voltage level is given by an external resistive driver, the current of this resistor must be cut so that it may be fixed to floating or VSS level, prior to or concurrently with causing the NT7538 to go to the sleep mode or standby mode.
- When an external power supply is used, likewise, the function of this external power supply must be stopped so that it may be fixed to floating or VSS level, prior to or concurrently with causing the NT7538 to go to the sleep mode or standby mode.

21. NOP

Non-Operation Command.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
	/RD	/WR									
0	1	0	1	1	1	0	0	0	1	1	E3h

22. Test Command

This is the dedicated IC chip test command. It must not be used for normal operation. If the Test command is issued inadvertently, set the /RES input to low or issue the Reset command to release the test mode.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
	/RD	/WR									
0	1	0	1	1	1	1	0	1	0	0	F0h to FFh

*: Invalid bit

Cautions: The NT7538 maintains an operation status specified by each command. However, the internal operation status may be changed by a high level of ambient noise. Users must consider how to suppress noise on the package and system or to prevent ambient noise insertion. To prevent a spike in noise, built-in software for periodical status refreshment is recommended. The test command can be inserted in an unexpected place. Therefore it is recommended to enter the test mode reset command F0h during the refresh sequence.

23. Oscillation Frequency Select

This command is to select the oscillation frequency of driver IC as below.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Oscillation Frequency
	/RD	/WR										
0	1	0	1	1	1	0	0	1	0	0	E4h	Typical 31.4 KHz
										1	E5h	Typical 26.3 KHz

24. Partial Display Mode Set

This command enables to select the display mode. When D0 is low, the IC is in normal display mode, the maximum display duty ratio is decided by pin connection of DUTY0 and DUTY1 and the command LCD Bias Set decides the LCD bias ratio. The IC enters into partial display mode when D0 is high, then the commands Partial Display Duty Set and Partial Display Bias Set decide the LCD display duty and bias ratios.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Display Mode
	/RD	/WR										
0	1	0	1	0	0	0	0	0	1	0	82h	Normal Display
										1	83h	Partial Display

25. Partial Display Duty and Bias Set

These two commands set the LCD display duty and bias ratios when the IC is in partial display mode. They are invalid when the IC is in normal display mode. When the partial display duty is set, the LCD bias for partial display is set simultaneous as below. The partial display duty will be kept at maximum duty (decided by pins DUTY0 and DUTY1) when setting duty is larger than maximum duty.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Partial Duty	Scanning Line
0	1	0	0	0	1	1	0	0	0	0	30h	1/9 duty	Line [0:7], COMS
								0	0	1	31h	1/17 duty	Line [0:15], COMS
								0	1	0	32h	1/33 duty	Line [0:31], COMS
								0	1	1	33h	1/49 duty	Line [0:47], COMS
								1	0	0	34h	1/65 duty	Line [0:63], COMS
								1	0	1	35h	Reserved	No effect
								1	1	*	37h	Reserved	No effect

Using Partial Display Bias Set command to change the LCD bias in partial display mode.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex	LCD Bias
0	1	0	0	0	1	1	1	0	0	0	38h	1/4
								0	0	1	39h	1/5
								0	1	0	3Ah	1/6
								0	1	1	3Bh	1/7
								1	0	0	3Ch	1/8
								1	0	1	3Dh	1/9
								1	1	0	3Eh	Reserved
								1	1	1	3Fh	Reserved

Note: The COM waveform of no display area is non-select waveform.

26. Partial Start Line Set (Double Byte Command)

This command makes it possible to set the partial start line for partial display. It is a two-byte command used as a pair and the Number of Start Line Set command must be issued after the Partial Start Line Set command.

(1) Partial Start Line Set

When this command is input, no other command except for the Number of Start Line Set command can be used.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	1	0	1	0	0	1	1	D3h

(2) Number of Start Line Set

By using this command to set six bits of data to the Partial Start Line register. Once the Number of the Start Line Set command has been used to set data into the register, then the partial start line will affect on the LCD display. The number of partial start line is always equal to zero when the partial start line is larger than maximum duty ratio (decided by pins DUTY0 and DUTY1).

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Partial Start Line
0	1	0	*	*	0	0	0	0	0	0	XX	0 line
					0	0	0	0	0	1	XX	1 line
					0	0	0	0	1	0	XX	2 line
								:			:	:
					1	1	1	1	1	0	XX	62 line
					1	1	1	1	1	1	XX	63 line

27. The N-Line Inversion (Double Byte Command)

This command makes it possible to adjust the number of scan lines for liquid crystal display inversion. It is a two-byte command used as a pair and the Number of Line Set command must be issued after the N-Line Inversion Set command.

(1) N-Line Inversion Set

When this command is input, no other command except for the Number of Line Set command can be used.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
	/RD	/WR									
0	1	0	1	0	0	0	0	1	0	1	85h

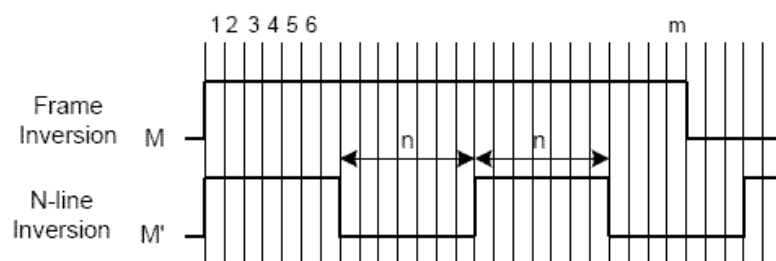
(2) Number of Line Set

By using this command to set five bits of data to the N-Line inversion register. Once the Number of Line Set command has been used to set the data into the register, then the N-Line inversion will affect on the LCD display.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Line Inversion
	/RD	/WR										
0	1	0	*	*	*	0	0	0	0	0	XX	1 line
						0	0	0	0	1	XX	2 line
											:	:
						1	1	1	1	1	XX	32 line

Note 1: The number of inversed scan line = register setting value + 1.

Note 2: When Partial Duty = 1/9 or 1/17, the N-line inversion function release and the LCD display scan line is back to frame inversion status.



28. Release N-Line Inversion

This command is used to exit the N-Line inversion function. The N-Line inversion function is released and the LCD display is set back to frame inversion status once this command is executed.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
	/RD	/WR									
0	1	0	1	0	0	0	0	1	0	0	84h

29. DC/DC Clock Frequency (Double Byte Command)

This command makes it possible to adjust the frequency for DC/DC clock. It is a two-byte command used as a pair and the DC/DC Frequency Division Set command must be issued after the DC/DC Clock Set command.

(1) DC/DC Clock Set

When this command is input, no other command except for the DC/DC Frequency Division Set command can be used.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	1	1	0	0	1	1	0	E6h

(2) DC/DC Frequency Division Set

By using this command to set five bits of data to the frequency division register.

A0	E	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Division
0	1	0	*	*	*	*	0	0	0	0	XX	fOSC
							0	0	0	1	XX	fOSC/2
							0	0	1	0	XX	fOSC/4
							0	0	1	1	XX	fOSC/6 (default)
							0	1	0	0	XX	fOSC/8
							0	1	0	1	XX	fOSC/10
							0	1	1	0	XX	fOSC/12
							0	1	1	1	XX	fOSC/14
							1	0	0	0	XX	fOSC/16
							1	0	0	1	XX	fOSC/18
							1	0	1	0	XX	fOSC/20
							1	0	1	1	XX	fOSC/22
							1	1	0	0	XX	fOSC/24
							1	1	0	1	XX	fOSC/26
							1	1	1	0	XX	fOSC/28
							1	1	1	1	XX	fOSC/30

Table 14. Command Table

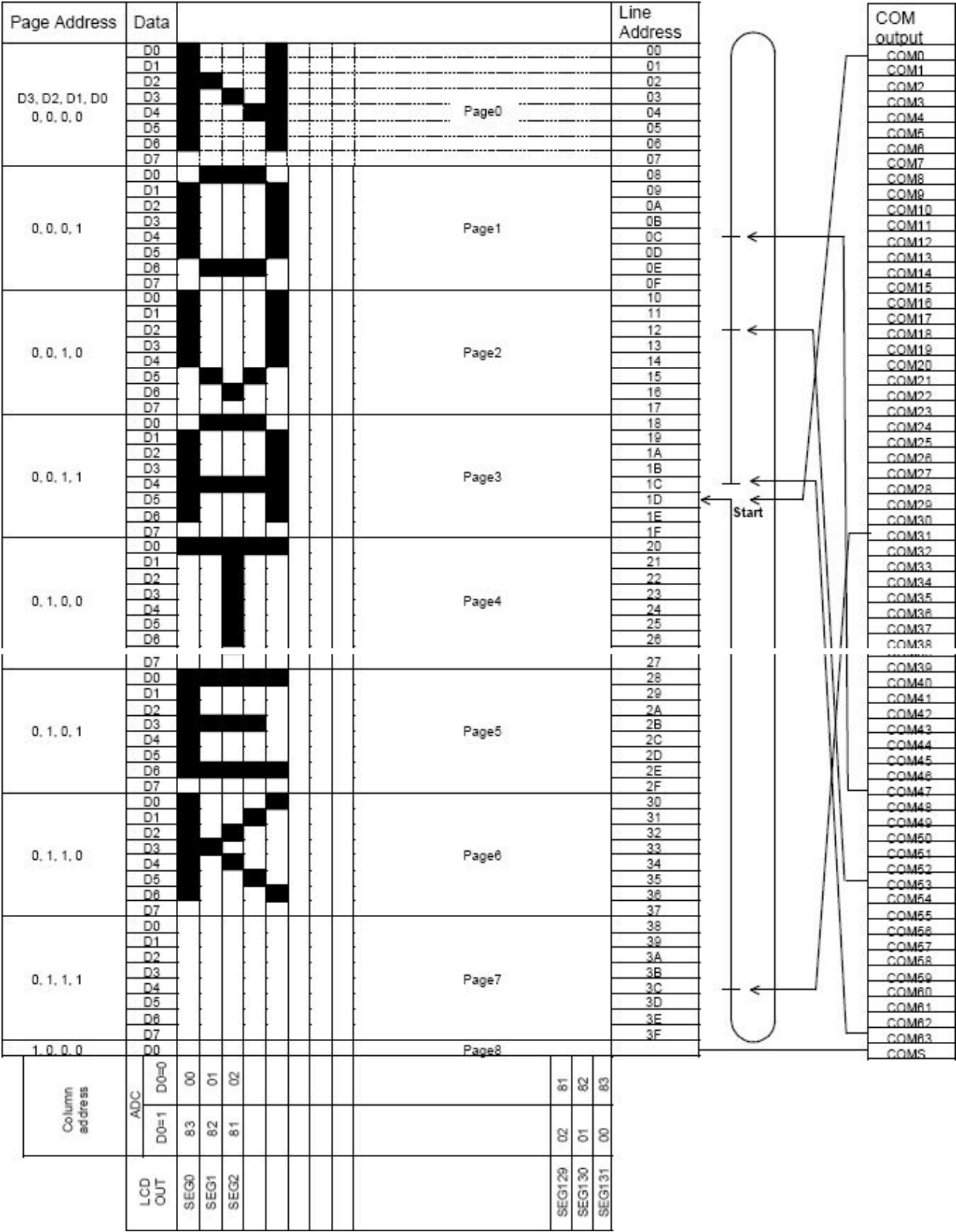
Command	A0	/RD	/WR	Code									Hex	Function
				D7	D6	D5	D4	D3	D2	D1	D0			
(1) Display OFF	0	1	0	1	0	1	0	1	1	1	0	1	AEh AFh	Turn on LCD panel when high, and turn off when low
(2) Display Start Line Set	0	1	0	0	1	Display Start Address						40h to 7Fh	Specifies RAM display line for COM0	
(3) Page Address Set	0	1	0	1	0	1	1	Page Address				B0h to B8h	Set the display data RAM page in Page Address register	
(4) Column Address Set	0	1	0	0	0	0	1	Higher Column Address				00h to 18h	Set 4 higher bits and 4 lower bits of column address of display data RAM in register	
	0	1	0	0	0	0	0	Lower Column Address						
(5) Read Status	0	0	1	Status				0	0	0	0	XX	Reads the status information	
(6) Write Display Data	1	1	0	Write Data								XX	Write data in display data RAM	
(7) Read Display Data	1	0	1	Read Data								XX	Read data from display data RAM	
(8) ADC Select	0	1	0	1	0	1	0	0	0	0	0	1	A0h A1h	Set the display data RAM address SEG output correspondence
(9) Normal/Reverse Display	0	1	0	1	0	1	0	0	1	1	0	1	A6h A7h	Normal indication when low, but full indication when high
(10)Entire Display ON/OFF	0	1	0	1	0	1	0	0	1	0	0	1	A4h A5h	Select normal display (0) or entire display on
(11)LCD Bias Set	0	1	0	1	0	1	0	0	0	1	0	1	A2h A3h	Sets LCD driving voltage bias ratio
(12)Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	0	E0h	Increments column address counter during each write
(13)End	0	1	0	1	1	1	0	1	1	1	0	0	EEh	Releases the Read-Modify-Write
(14)Reset	0	1	0	1	1	1	0	0	0	1	0	0	E2h	Resets internal functions
(15)Common Output Mode Select	0	1	0	1	1	0	0	0	1	*	*	*	C0h to CFh	Select COM output scan direction *: invalid data
(16)Power Control Set	0	1	0	0	0	1	0	1	Operation Status			28h to 2Fh	Select the power circuit operation mode	
(17)V0 Voltage Regulator Internal Resistor ratio Set	0	1	0	0	0	1	0	0	Resistor Ratio			20h to 27h	Select internal resistor ratio Rb/Ra mode	
(18)Electronic Volume mode Set Electronic Volume Register Set	0	1	0	1	0	0	0	0	0	0	0	1	81h	
	0	1	0	*	*	Electronic Control Value						XX	Sets the V0 output voltage electronic volume register	
(19)Set Static indicator ON/OFF Set Static Indicator Register	0	1	0	1	0	1	0	1	1	0	0	1	ACh ADh	Sets static indicator ON/OFF 0: OFF, 1: ON
	0	1	0	*	*	*	*	*	*	Mode		XX	Sets the flash mode	
(20)Power Save	0	1	0	-	-	-	-	-	-	-	-	-	-	Compound command of Display OFF and Entire Display ON
(21)NOP	0	1	0	1	1	1	0	0	0	1	1	1	E3h	Command for non-operation

Command Table (continue)

Command	A0	/RD	/WR	Code								Hex	Function
				D7	D6	D5	D4	D3	D2	D1	D0		
(22)Oscillation Frequency Select	0	1	0	1	1	1	0	0	1	0	0 1	E4h E5h	Select the oscillation frequency
(23)Partial Display mode Set	0	1	0	1	0	0	0	0	0	1	0 1	82h 83h	Enter/Release the partial display mode
(24)Partial Display Duty Set	0	1	0	0	0	1	1	0	Duty Ratio			30h 37h	Sets the LCD duty ratio for partial display mode
(25)Partial Display Bias Set	0	1	0	0	0	1	1	1	Bias Ratio			38h 3Fh	Sets the LCD bias ratio for partial display mode
(26)Partial Start Line Set	0	1	0	1	1	0	1	0	0	1	1	D3h	Enter Partial Start Line Set
Partial Start Line Set	0	1	0	1	1	Partial Start Line						XX	Sets the LCD Number of partial display start line
(27)N-Line Inversion Set	0	1	0	1	0	0	0	0	1	0	1	85h	Enter N-Line inversion
Number of Line Set	0	1	0	*	*	*	Number of Line					XX	Sets the number of line used for N-Line inversion
(28)N-Line Inversion Release	0	1	0	1	0	0	0	0	1	0	0	84h	Exit N-Line Inversion
(29)DC/DC Clock Set	0	1	0	1	1	1	0	0	1	1	0	E6h	Set DC/DC Clock Frequency
DC/DC Clock Division Set	0	1	0	1	1	0	0	Clock Division				XX	Set the Division of DC/DC Clock Frequency
(30)Test Command	0	1	0	1	1	1	1	*	*	*	*	F1h to FFh	IC test command. Do not use!
(31)Test Mode Reset	0	1	0	1	1	1	1	0	0	0	0	F0h	Command of test mode reset

Note: Do not use any other command, or system malfunction may result.

Figure 4. Relationship between display data RAM and address. (if initial display line is 1DH)



6. 质量标准

6.1 合格质量标准

检验项目	检测标准	AQL
电气特性	GB2828-81 检测水平 II 常规检测 单个样品检测	0.65
非电气特性	GB2828-81 检测水平 II 常规检测 单个样品检测	1.5
尺寸测量	GB2828-81 检测水平 II 常规检测 单个样品检测	1.5

6.2 检验环境条件

- 室温: $25 \pm 3^{\circ}\text{C}$
- 湿度: $65 \pm 20\%\text{RH}$

6.3 检验标准

6.3.1 加电检测

检测项目	检测标准
无显示	任何像素有不显示的情况，视为不合格品
显示错误	不允许不当操作 在所选择模式，出现异常显示或显示位置不正确
显示不正常	任何一列显示不正常，视为不合格品
过流	总电流要求与LCD所需电流相匹配，不允许超过LCD正常工作的最大电流值.
视角	视角不要接近规格书所标最小值，如果有接近最小值的产品做不合格品处理.
对比度	对比度不要接近规格书所标最小值，如果有接近最小值的产品做不合格品处理.
LCD驱动电压	见产品规格书

6.3.2 不加电检测

检测项目	检测标准
LCD尺寸	见LCD外形图，尺寸不允许超出公差范围
LCD面板划伤	如果有效区的划伤长和宽尺寸大于下面所示组合，我们做不合格处理。 数目：一个或更多 宽度：0.1 长度：3.0 三个或更多 宽度：0.05 长度：2.0 三个或更多 宽度：0.03 长度：3.0 当损坏超出这些尺寸，按不合格品处理。

7. 可靠性

测试项目	测试条件	备注
高温存储	70 °C,12hr.	2
低温存储	-20 °C,4hr	2
湿度存储	40 °C,90~95%RH,96hr	1、2
高温运行	40°C, 典型运行条件,48hr	
低温运行	0°C, 典型运行条件,48hr	

备注1：在LCD上不允许有任何水珠。

备注2：LCD应该在正常条件下储存4小时后进行检测。

条件 (15~35 °C,45~65%RH)

8. 出厂测试报告

(VDD=+3.0V ,Ta=25°C)

项目	条件	检测结果	备注
高温存储	80°C,120 hrs	无异常	---
低温存储	- 30°C,120 hrs	无异常	---
高温运行	70°C,240 hrs	无异常	---
低温运行	- 20°C,240 hrs	无异常	---
高温湿存储	50°C,90% RH,120 hrs	无异常	---
高温湿运行	40°C,90% RH,120 hrs	无异常	---

9. 注意事项

9.1 使用过程中注意事项

- (1) LCD 由两片带有偏光片的薄玻璃组装而成，必须避免剧烈震动、冲击、挤压和从高处掉落。

- (2) LCD 中的液晶材料是有害物质,当不慎溅落到手,身体,衣服等处时,应尽快用肥皂冲洗干净。
- (3) 请不要在 LCD 屏表面或屏周围施加有过大的挤压力,因为这样有可能引起屏色彩变化。
- (4) 贴在屏表面的偏光片很容易被划伤,所以我们在对 LCD 操作时必须注意,避免划伤。

9.2 LCD 处理及清洗注意事项

在清理 LCD 表面时,使用带溶剂(建议如下)的软布,轻轻擦拭。

- (1) 异丙醇
- (2) 乙醇
- (3) 不要用干燥或者比较硬的材料擦拭显示屏表面,否则很容易损坏表面偏光片。

以下溶剂请不要使用:

- (1) 水
- (2) 酮
- (3) 芳烃

9.3 严防静电

- (1) 在操作 LCD 时,要始终保持操作人充分接地. 使人体和液晶模块保持同一电位。
- (2) 液晶模块表面都有一层保护膜, 目的在于避免造成 LCD 的偏光片划伤,沾染污渍等. 请慢慢揭去液晶显示模块保护膜.如果快速揭去保护膜都将产生静电.
- (3) 注意厂房的湿度: 厂房湿度范围: 50~60%RH

9.4 设计注意事项

在设计 LCD 模组时,不允许超出 LCD 所规定的各项参数的极限值:

- (1) 任何一项参数超出 LCD 所规定的参数值,都有可能影响显示效果。
- (2) LCD 工作温度应在规定范围之内, 如果超出 LCD 工作温度范围, 将影响显示效果。
- (3) 我们建议电源线有过流保护线。
- (4) 务必要注意周围设备所产生的干扰。
- (5) 如果要将 LCD 屏装入模组, 请固定牢 LCD 屏。

9.5 操作注意事项

- (1) LCD 如果输入电压过高会缩短它的寿命,所以对 LCD 的输入电压进行限制是很重要的。
- (2) LCD 在低温运行时响应时间相对于正常工作温度将明显变慢, 另一方面, 在高温环境运行 LCD 屏将变黑。但是, 这些现象并不意味着模块故障或 LCD 失控, 当温度调整到正常工作范围时, 模块工作恢复正常。
- (3) 终端如果有轻微裸露都将引起电化学反应导致终端开路。

(5) 如果工作温度在最高工作温度, 那么要求湿度小于等于 50%RH.

9.6 焊接注意事项:

在焊接 LCD 屏 FPC 时须注意以下几点:

※ LCD 屏上只有 FPC 焊接处可以焊接.

※ 焊接所需的烙铁必须绝缘.

焊接时所需条件:

电铁的温度: $280^{\circ}\text{C} \pm 10^{\circ}\text{C}$

焊接时间: $< 3-4\text{S}$

焊接材料: 低熔点, 可充分熔化的焊锡。

9.7 包装与存储

当 LCD 屏需要长时间储存时, 应遵循以下原则: 如果储存方法不当, 将影响偏光片的质量, 使显示效果不佳;

- (1) 储存时尽可能使用出厂时的原包装.
- (2) 储存散装的 LCD 时, 应先装入防静电袋, 封口严密.
- (3) 为防止屏性能退化, 不要暴露在高湿温环境或有阳光直射的位置对它直接操作或存储。
- (4) 储存应保持低湿度, 最佳储存温度范围为: $0^{\circ}\text{C} \sim 35^{\circ}\text{C}$
- (5) 存储时不允许任何东西接触到偏光片表面。

10. 使用须知

(1) 在合作双方认为有必要提供定制样品的情况下应该提供样品。合同在样品设计好并且双方确认后生效。

(2) 在遇到以下情况, 必须经双方代表讨论并且同意后处理问题:

- 当产品规格书出现问题时。
- 当一个新的问题出现, 而在此产品规格书中没有说明时。
- 如果客户的检测标准或运行条件改变要告知清达, 这些改变将使产品规格书出现问题。
- 当一个新的问题在客户操作过程中出现, 经分析样品也存在该问题时。